CLAIMS

1. (previously amended) A chip rate base band processor which receives digital information containing symbol information and provides a symbol output, comprising:

an input memory which stores the digital information;

a data PN code buffer;

a pilot PN code buffer;

a pilot multiplier having a first input coupled to the pilot PN code buffer, a second input coupled to the input memory, and an output;

a data multiplier having a first input coupled to the data PN code buffer, a second input coupled to the input memory, and an output;

a pilot correlator having an input coupled to the output of the first multiplier, and an output;

a pilot memory coupled to the pilot correlator;

a channel estimator coupled to the pilot memory;

a peak detector coupled to the pilot memory;

a data correlator coupled to the data multiplier;

load controller having a first input coupled to the peak detector, a second input coupled to data correlator, and an output;

a data memory coupled to the load controller;

a phase rotator having a first input coupled to the channel estimator, a second input coupled to the data memory, and an output; and

a symbol combiner having an input coupled to the phase rotator, and an output which provides the symbol output.

2. (original) The chip rate base band processor of claim 1 further comprising a cluster tracker having an input coupled to the pilot memory, and an output coupled to the pilot PN code buffer.

3. (original) The chip rate base band processor of claim 1 wherein the output of the cluster tracker is coupled to the data PN code buffer.

4-19. (cancelled).